

# UBA2212

## Half-bridge power IC family for CFL lamps

Rev. 3 — 27 February 2012

Product data sheet

## 1. General description

---

The UBA2212 family of integrated circuits are a range of high voltage monolithic ICs for driving Compact Fluorescent Lamps (CFL) in half-bridge configurations. The family is designed to provide easy integration of lamp loads across a range of burner power and mains voltages.

## 2. Features and benefits

---

### 2.1 System integration

- Integrated half-bridge power transistors
  - ◆ UBA2212C: 120 V; 2  $\Omega$ ; 3.5 A maximum ignition current
- Integrated bootstrap diode
- Integrated high-voltage supply

### 2.2 General

- RMS lamp current control

### 2.3 Fast and smooth light out

- Boost with externally controlled timing
- Temperature controlled timing during boost state
- Smooth transition from boost to steady state

### 2.4 Burner lifetime

- Fixed frequency preheat with adjustable preheat time
- Minimum glow time control to support cold start
- Lamp power independent from mains voltage variations
- Lamp inductor saturation protection during ignition



## 2.5 Safety

- Saturation Current Protection (SCP)
- OverTemperature Protection (OTP)
- Capacitive Mode Protection (CMP)

## 2.6 Ease of use

- Adjustable operating frequency for easy fit with various burners

## 3. Applications

- Compact Fluorescent Lamps up to 23 W for 120 V (AC) indoor and outdoor applications

## 4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UBA2212CP/1	DIP14	plastic dual inline package; 14 leads (300 mil)	SOT27-1
UBA2212CT/1	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

5. Block diagram

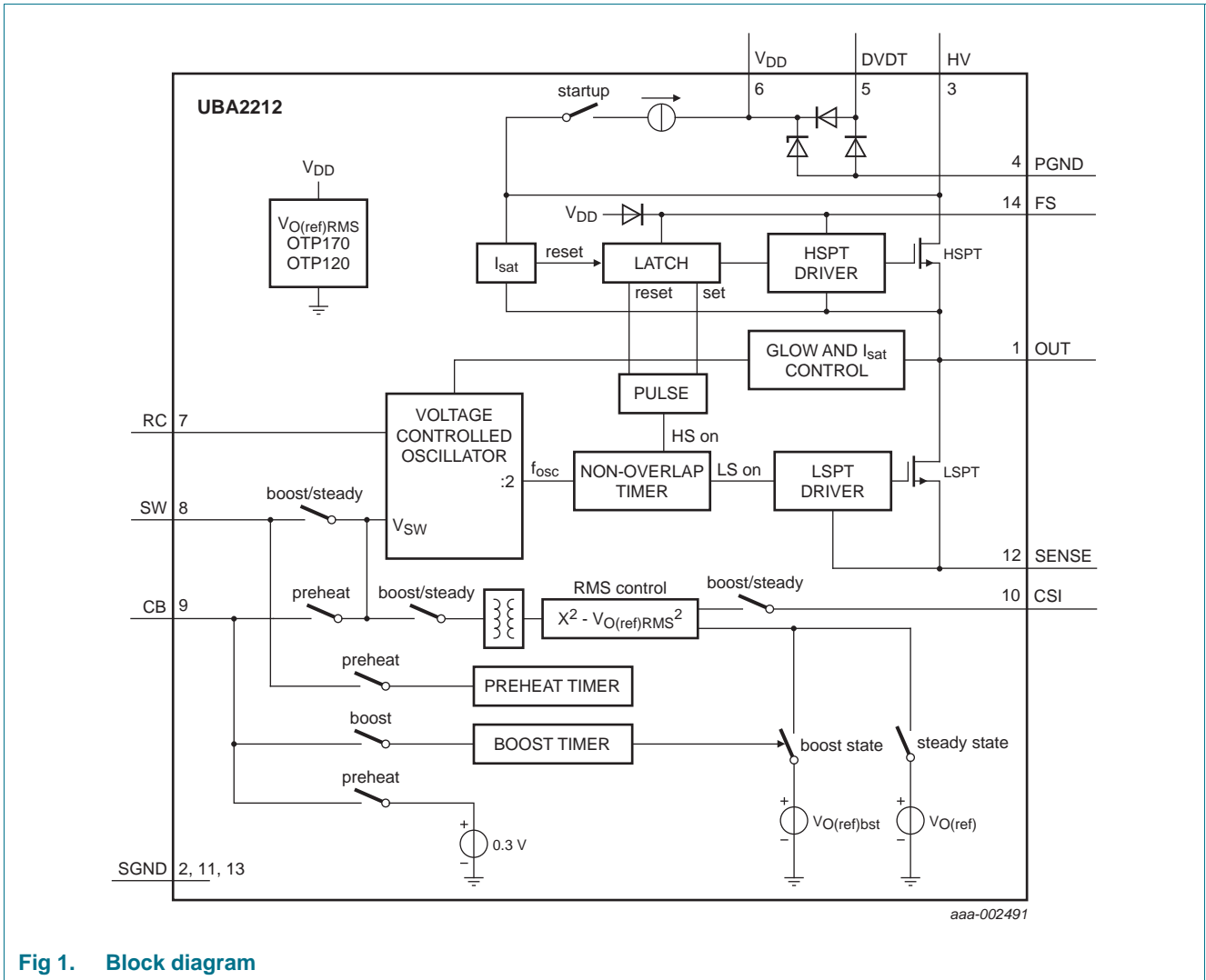


Fig 1. Block diagram

## 6. Pinning information

### 6.1 Pinning

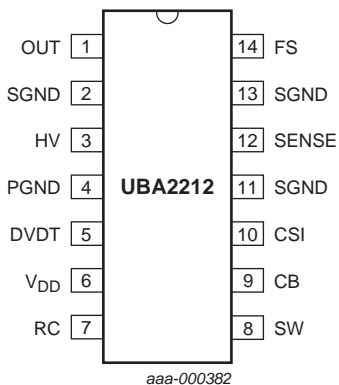


Fig 2. Pin configuration for UBA2212CP (SOT27-1)

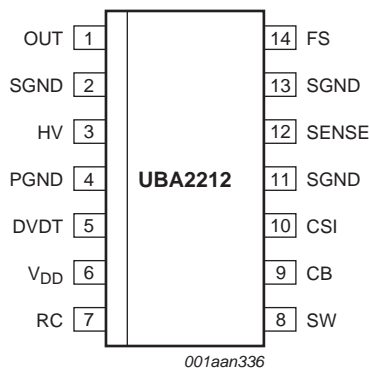


Fig 3. Pin configuration for UBA2212CT (SOT108-1)

### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
OUT	1	half-bridge output
SGND	2, 11, 13	signal ground
HV	3	high-voltage supply
PGND	4	DVDT supply ground
DVDT	5	DVDT supply input
V <sub>DD</sub>	6	internal low-voltage supply output
RC	7	internal oscillator input
SW	8	sweep timing and VCO input
CB	9	boost timing capacitor/preheat integrating capacitor
CSI	10	current feedback sense input
SENSE	12	current sense of LS MOSFET
FS	14	high-side floating supply output

## 7. Functional description

### 7.1 Supply voltage

The UBA2212 family is powered using a start-up current source and a DVDT supply. When the voltage on pin HV increases, the  $V_{DD}$  capacitor ( $C_{VDD}$ ) is charged using the internal Junction gate Field-Effect Transistor (JFET) current source. The voltage on pin  $V_{DD}$  rises until  $V_{DD}$  equals  $V_{DD(start)}$ . The start-up current source is then disabled. The half-bridge starts switching causing the charge pump to generate the required  $V_{DD}$  supply.

The amount of current flowing towards  $V_{DD}$  equals  $V_{HV} \times C_{DVDT} \times f$  where  $f$  represents the momentary frequency. The charge pump consists of an external half-bridge capacitor ( $C_{DVDT}$ ). The IC contains two internal diodes with an internal Zener diode. The Zener diode ensures the  $V_{DD}$  voltage cannot rise above the maximum  $V_{DD}$  rating.

The DVDT supply has its own ground pin (PGND) to prevent large peak currents from flowing through the external small signal ground pin (SGND).

The start-up current source is enabled when the voltage on pin  $V_{DD}$  is below  $V_{DD(stop)}$ .

### 7.2 Start-up state

When the supply voltage on pin  $V_{DD}$  increases, the IC enters the start-up state. In the start-up state, the High-Side Power Transistor (HSPT) is switched off and the Low-Side Power Transistor (LSPT) is switched on. The circuit is reset and the capacitors on the bootstrap pin FS ( $C_{bs}$ ) and the low-voltage supply pin  $V_{DD}$  ( $C_{VDD}$ ) are charged. Pins RC and SW are switched to ground.

When pin  $V_{DD}$  is above  $V_{DD(start)}$ , the start-up state is exited and the preheat state is entered. If the voltage on pin  $V_{DD}$  falls below  $V_{DD(stop)}$ , the system returns to the start-up state.

**Remark:** If OTP is active, the IC remains in the start-up state for as long as this is the case. The  $V_{DD}$  voltage slowly oscillates between  $V_{DD} = V_{DD(stop)}$  and  $V_{DD} = V_{DD(start)}$ .

### 7.3 Reset

A DC reset circuit is incorporated in the high-side driver. The high-side transistor is switched off when the voltage on pin FS is below the high-side lockout voltage.

### 7.4 Oscillation control

The oscillation frequency is based on the 555-timer function. A self oscillating circuit is created comprising the external components: resistors  $R_{osc}$ ,  $R_{sense}$  and capacitor  $C_{osc}$ .  $R_{osc}$  and  $C_{osc}$  determine the nominal oscillating frequency.

An internal divider  $0.5 \times f_{osc(int)}$  is used to generate the accurate 50 % duty cycle. The divider sets the bridge frequency at half the oscillator frequency.

The input on pin SW generates signal  $V_{SW}$ . The  $V_{SW}$  signal is used to determine the frequency in all states except preheat. Signal  $V_{CB}$  is an internally generated signal used to determine the frequency during the preheat state.

The output voltage of the bridge changes with the falling edge of the signal on pin RC. The nominal half-bridge frequency is shown in [Equation 1](#):

$$f_{osc(nom)} = \frac{I}{k_{osc} \times R_{osc} \times C_{osc}} \tag{1}$$

The maximum frequency is  $2.5 \times f_{osc(nom)}$  and is set at  $V_{SW}$ . An overview of the oscillator, internal LSPT and HSPT drive signals and the output is shown in [Figure 4](#).

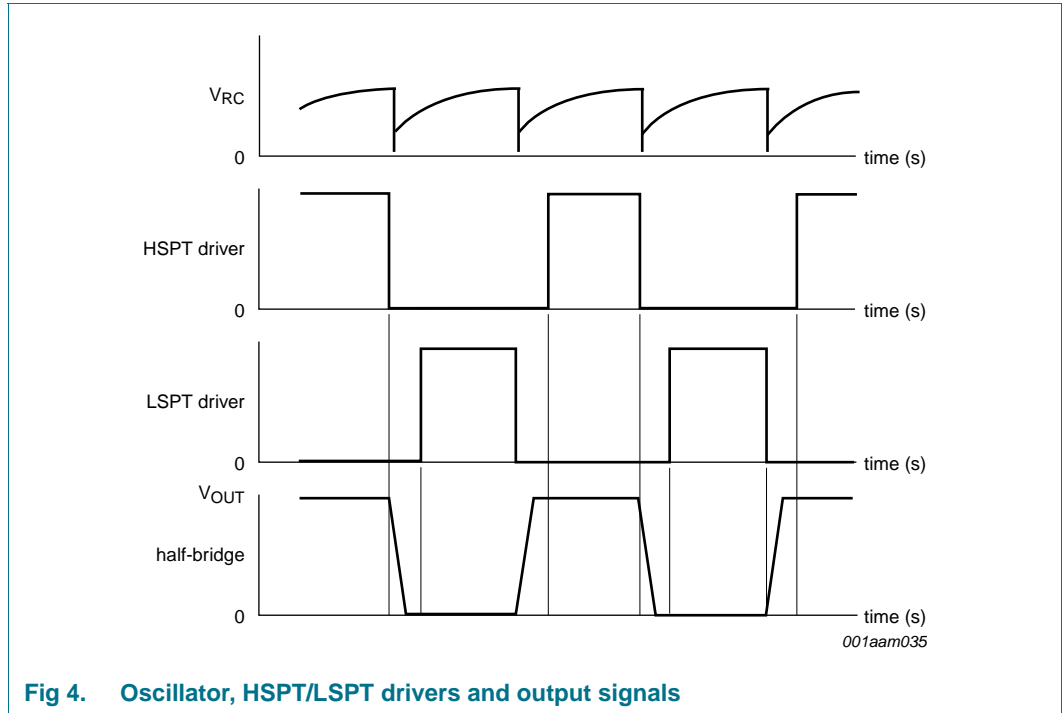


Fig 4. Oscillator, HSPT/LSPT drivers and output signals

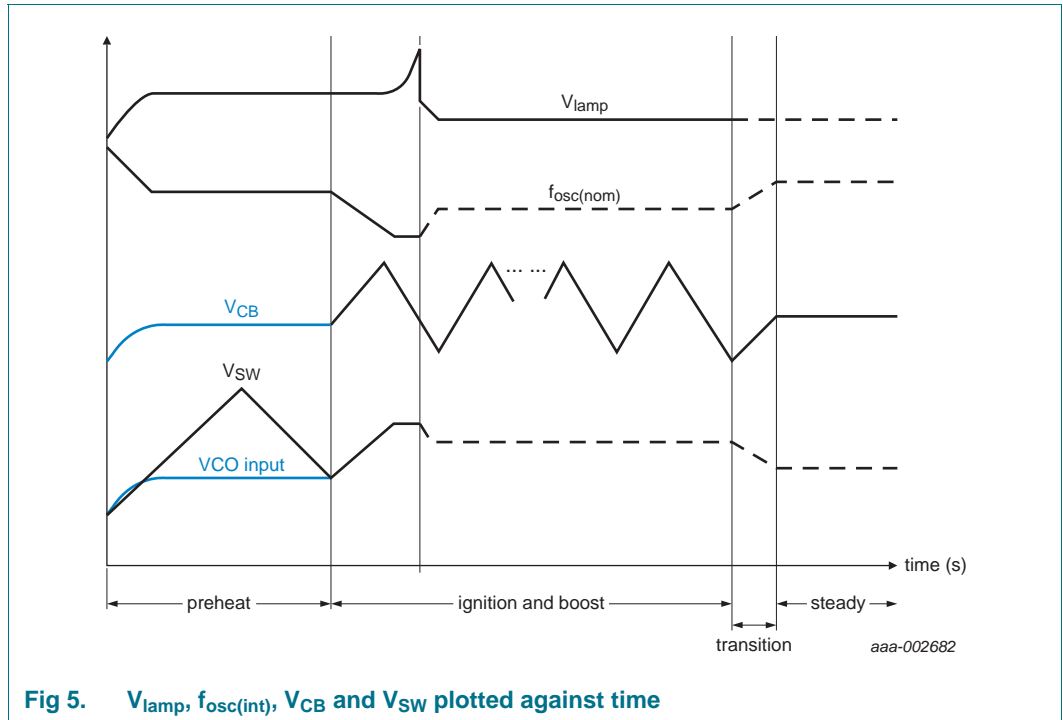
### 7.5 Preheat state

The VCO input is directly connected to a fixed DC voltage of 0.3 V in the preheat state. The frequency is set to about  $0.94 f_{max}$  to ensure voltage mode preheat. The preheat state is finished when  $V_{SW}$  drops to 0.3 V.

### 7.6 Ignition state

The ignition state is entered after the preheat state has finished. Current  $I_{SW}$  charges the capacitor on pin SW ( $C_{SW}$ ) and the frequency continuously drops.

During this frequency sweep ( $f_{SW}$ ), the resonance frequency is reached resulting in the ignition of the lamp (see [Figure 5](#)). The lamp inductor ( $L_{lamp}$ ) and lamp capacitor ( $C_{lamp}$ ) set the resonance frequency.



### 7.7 Boost state and transition to steady state

The boost state is entered after ignition. The output of RMS current control circuit and the input of VCO are switched to capacitor  $C_{SW}$ . At the same time, the input of RMS current control circuit is switched to pin CSI to sense lamp current. On pin CB, capacitor  $C_{CB}$  is connected to the boost timer input to control the boost time.  $V_{SW}$  changes to a given voltage to set the lamp current to the level pre-defined by the internal boost reference and resistor  $R_{CSI}$ . The calculation is shown in [Equation 2](#):

$$Boost I_{lamp} = \frac{V_{ref(bst)}}{R_{CSI}} \tag{2}$$

When boost timer gives a signal to indicate that boost state is ended, the transition from boost to steady state starts to avoid flicker. In this state, the boost transition timer is active to define the transition time, which is also realized with capacitor  $C_{CB}$  on CB pin.

### 7.8 Steady state

When the RMS current control circuit leaves the system operating at the normal lamp current, it enters the steady state. In this state, the voltage on pin CB is fixed and the voltage on pin SW is controlled by a feedback loop. This feature enables the lamp current to be independent of the mains or lamp voltage.

The same analysis as with the boost state can be used to express lamp current ([Equation 3](#)):

$$Steady I_{lamp} = \frac{V_{ref(steady)}}{R_{CSI}} \tag{3}$$

Therefore, the boost-steady ratio can be found as shown in [Equation 4](#):

$$\text{Boost to steady ratio} = \frac{V_{ref(bst)}}{V_{ref(steady)}} \quad (4)$$

## 7.9 Non-overlap time

The non-overlap time is defined as the time when both MOSFETs are not conducting. The non-overlap time is fixed internally and is fixed at the  $t_{no}$  value (see [Table 5](#)).

## 7.10 OverTemperature Protection (OTP)

OTP is active in all states except boost. When the die temperature reaches the OTP activation threshold ( $T_{th(act)otp}$ ), the oscillator is stopped and the power switches (LSPT/HSPT) are set to the start-up state. When the oscillator is stopped, the DVDT supply no longer generates the supply current  $I_{DVDT}$ . Voltage  $V_{DD}$  gradually decreases and the start-up state is entered as described in [Section 7.2 on page 5](#). OTP is reset when the temperature  $< T_{th(rel)otp}$ .

During boost state, the threshold of temperature is  $T_{j(end)bst}$  which is lower than  $T_{th(otp)}$ . When the die temperature has reached  $T_{j(end)bst}$ , the boost state ends, the IC enters steady state and OTP is enabled.

## 7.11 Saturation Current Protection (SCP)

A critical parameter in the design of the lamp inductor is its saturation current. When the momentary inductor exceeds its saturation current, the inductance drops significantly. The inductor current and the current flowing through the LSPT and HSPT power switches increases rapidly if this happens. The increase can cause the current to exceed the half-bridge power transistors maximum ratings.

Saturation of the lamp inductor is likely to occur in cost-effective and miniaturized CFLs. The UBA2212 family internally monitors the power transistor current. When this current exceeds the momentary rating of the internal half-bridge power transistors, the conduction time is reduced and the frequency is slowly increased (by discharging  $C_{SW}$ ). This function causes the system to balance at the edge of the current rating of the power switches.

## 7.12 Capacitive Mode Protection (CMP)

In boost and steady state,  $V_{SW}$  determines the operating frequency. The RMS current control circuit and the CMP circuit control this frequency. When Capacitive mode is detected, capacitor  $C_{SW}$  is mainly controlled by the CMP circuit. Capacitor  $C_{SW}$  is discharged by a current source, which is also dependent on the hard switching voltage level. The operating frequency  $f_{osc}$ , increases until CMP is no longer detected.

**Remark:** CMP always controls the operation. If the lamp current is lower than the defined value before CMP is detected, the system moves to the edge of hard switching (~25 V). The set value cannot be achieved. Change the LC tank to get a higher resonant gain, which enables the required lamp current to be obtained.



## 8. Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>HV</sub>	voltage on pin HV	operating	-	202	V
		mains transients during 0.5 s	-	250	V
V <sub>FS</sub>	voltage on pin FS		V <sub>HV</sub>	V <sub>HV</sub> + 14	V
V <sub>DD</sub>	supply voltage	DC supply	0	14	V
V <sub>SENSE</sub>	voltage on pin SENSE		-5	+5	V
V <sub>RC</sub>	voltage on pin RC	I <sub>RC</sub> < 1 mA	0	V <sub>DD</sub>	V
V <sub>SW</sub>	voltage on pin SW	I <sub>SW</sub> < 1 mA	0	V <sub>DD</sub>	V
I <sub>OUT</sub>	current on pin OUT	T <sub>j</sub> < 125 °C	-3.5	+3.5	A
I <sub>DVDT</sub>	current on pin DVDT	T <sub>j</sub> < 125 °C	-2.5	+2.5	A
V <sub>i(CSI)</sub>	input voltage on pin CSI	T <sub>j</sub> > -40 °C	-3.5	+3.5	V
SR	slew rate	repetitive output on pin OUT	-4	+4	V/ns
T <sub>j</sub>	junction temperature		-40	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+150	°C
T <sub>stg</sub>	storage temperature		-55	+150	°C
V <sub>ESD</sub>	electrostatic discharge voltage	Human Body Model (HBM): <a href="#">[1]</a>			
		pins HV, FS, OUT	-	800	V
		pins SW, RC, V <sub>DD</sub> , DVDT	-	2.5	kV
		Charged Device Model (CDM):			
		pins SW, RC, V <sub>DD</sub> , DVDT, CSI and CB	-	400	V

[1] In accordance with the Human Body Model (HBM): equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

## 9. Thermal characteristics

**Table 4. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
<b>DIP14 package</b>				
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	<a href="#">[1]</a> 70	K/W
R <sub>th(j-c)</sub>	thermal resistance from junction to case	in free air	<a href="#">[1]</a> 16	K/W
<b>SO14 package</b>				
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	<a href="#">[1]</a> 95	K/W
R <sub>th(j-c)</sub>	thermal resistance from junction to case	in free air	<a href="#">[1]</a> 16	K/W

[1] In accordance with IEC 60747-1

## 10. Characteristics

**Table 5. Characteristics**

$T_j = 25\text{ °C}$ ; all voltages are measured with respect to SGND; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Low-voltage supply</b>						
<b>Start-up state</b>						
$I_{HV}$	current on pin HV	$V_{HV} = 60\text{ V}$	-	1.5	-	mA
$V_{DD(start)}$	start supply voltage	oscillation start	11.5	12.5	13.5	V
$V_{DD(stop)}$	stop supply voltage	oscillation stop	8.5	9	9.5	V
$V_{DD(hys)}$	hysteresis of supply voltage	start – stop	3	3.5	4	V
$V_{DD(reg)}$	regulation supply voltage		-	12.5	-	V
$I_{sink}$	sink current	capability of VDD regulator	6	-	-	mA
<b>Output stage</b>						
$R_{on}$	on-state resistance	HS; $V_{HV} = 170\text{ V}$ ; $I_D = 200\text{ mA}$	-	2	-	$\Omega$
		LS; $V_{HV} = 170\text{ V}$ ; $I_D = 200\text{ mA}$	-	2	-	$\Omega$
$R_{on(150)}/R_{on(25)}$	on-state resistance ratio (150 °C to 25 °C)		-	1.4	-	
$V_{Fd}$	diode forward voltage	HS; $I_F = 320\text{ mA}$	-	1.1	-	V
		LS; $I_F = 320\text{ mA}$	-	1.2	-	V
		bootstrap diode; $I_F = 1\text{ mA}$	0.7	1	1.3	V
$t_{no}$	non-overlap time		0.9	1.2	1.5	$\mu\text{s}$
$V_{FS}$	voltage on pin FS	UnderVoltage LockOut with respect to pin OUT	3.9	4.5	5.1	V
$I_{FS}$	current on pin FS	$V_{HV} = 170\text{ V}$ ; $V_{FS} = 12\text{ V}$	10	14	18	$\mu\text{A}$
$I_{sat}$	saturation current	HS; $V_{DS} = 14\text{ V}$ ; $T_j \leq 125\text{ °C}$	3.5	-	-	A
		LS; $V_{DS} = 14\text{ V}$ ; $T_j \leq 125\text{ °C}$	3.5	-	-	A
<b>Internal oscillator</b>						
$f_{osc(min)}$	minimum oscillator frequency	$R_{osc} = 100\text{ k}\Omega$ ; $C_{osc} = 220\text{ pF}$ ; $V_{SW} = V_{DD}$	-	36	-	kHz
$f_{osc(max)}$	maximum oscillator frequency	$R_{osc} = 100\text{ k}\Omega$ ; $C_{osc} = 220\text{ pF}$ ; $V_{SW} = 0\text{ V}$	-	104	-	kHz
$\Delta f_{osc(nom)}/\Delta T$	nominal oscillator frequency variation with temperature	$R_{osc} = 100\text{ k}\Omega$ ; $C_{osc} = 220\text{ pF}$ ; $\Delta T = -20\text{ to }+150\text{ °C}$	-	2	-	%
$k_H$	high-level trip point factor		0.36	0.38	0.50	
$k_L$	low-level trip point factor		0.018	0.029	0.040	
$V_{H(RC)}$	HIGH-level voltage on pin RC	trip point; $V_{H(RC)} = k_H \times V_{DD}$	4.45	4.78	5.20	V
$V_{L(RC)}$	LOW-level voltage on pin RC	trip point; $V_{L(RC)} = k_L \times V_{DD}$	0.255	0.362	0.455	V
$K_{osc}$	oscillator constant	$R_{osc} = 100\text{ k}\Omega$ ; $C_{osc} = 220\text{ pF}$	1.065	1.1	1.135	
<b>Preheat function</b>						
$t_{ph}$	preheat time	$C_{SW} = 47\text{ nF}$	-	0.55	-	s
$f_{ph}$	preheat frequency	$R_{osc} = 100\text{ k}\Omega$ ; $C_{osc} = 220\text{ pF}$	-	90	-	kHz
$V_{RC}$	voltage on pin RC	trip point during preheat state	-	0.3	-	V

**Table 5. Characteristics ...continued** $T_j = 25\text{ °C}$ ; all voltages are measured with respect to SGND; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Boost function</b>						
$V_{O(\text{ref})\text{bst}}$	boost reference output voltage	$V_{DD} = 12\text{ V}$ ; $H_V = 30\text{ V}$ ; $V_{SW} = 3\text{ V}$	-	450	-	mV
$T_{j(\text{end})\text{bst}}$	boost end junction temperature		-	90	-	°C
$t_{\text{bst}}$	boost time	$C_{SW} = 220\text{ nF}$	-	48	-	s
$t_t$	transition time	$C_{SW} = 220\text{ nF}$	-	2	-	s
<b>Steady function</b>						
$V_{O(\text{ref})}$	steady reference output voltage	$V_{DD} = 12\text{ V}$ ; $H_V = 30\text{ V}$ ; $V_{SW} = 3\text{ V}$	-	300	-	mV
$N_{\text{LCBR}}$	lamp current boost ratio	boost and steady state	-	1.5	-	
<b>OTP function</b>						
$T_{\text{th}(\text{act})\text{otp}}$	overtemperature protection activation threshold temperature		-	170	-	°C
$T_{\text{th}(\text{rel})\text{otp}}$	overtemperature protection release threshold temperature		-	100	-	°C



## 12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

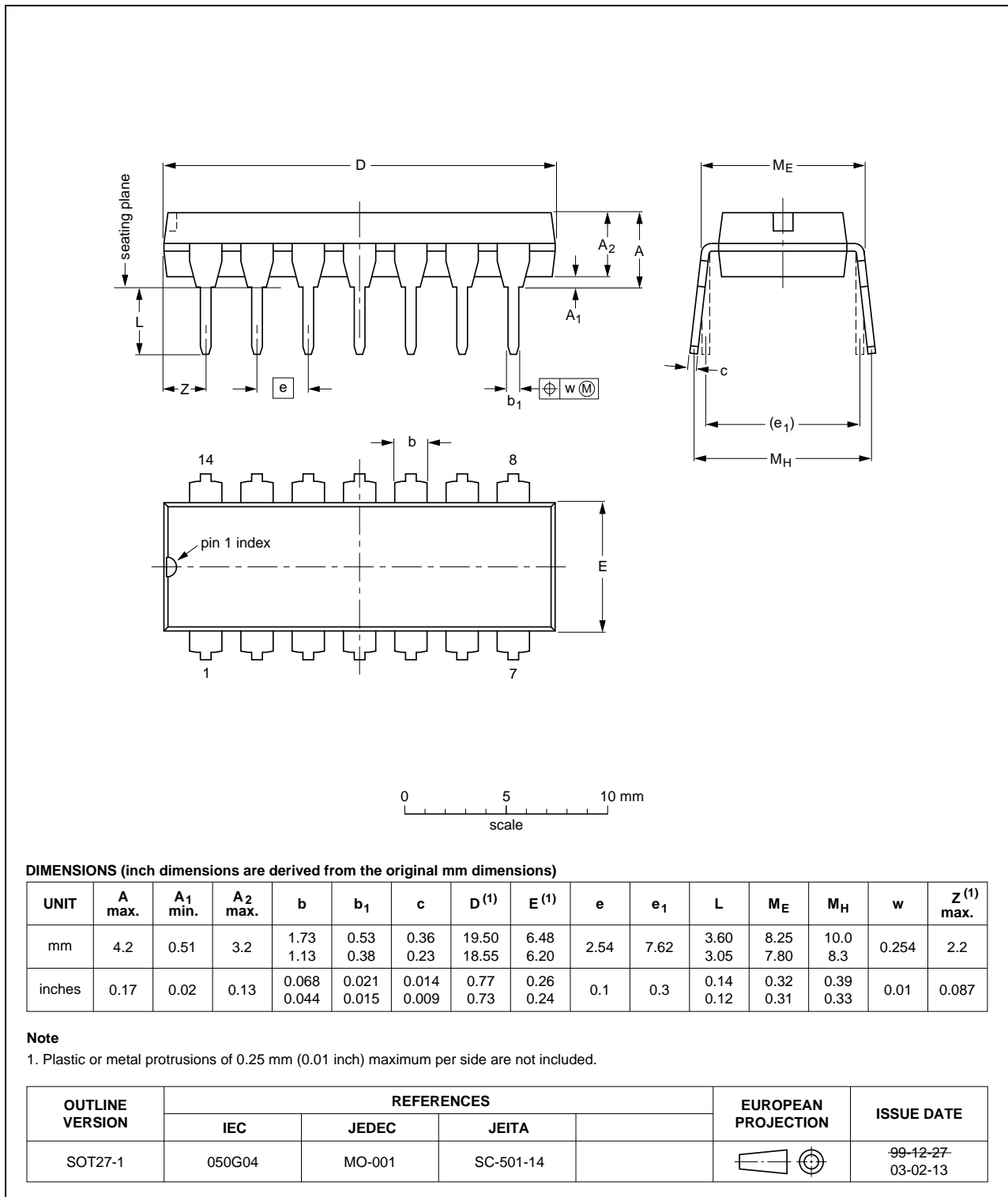


Fig 7. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

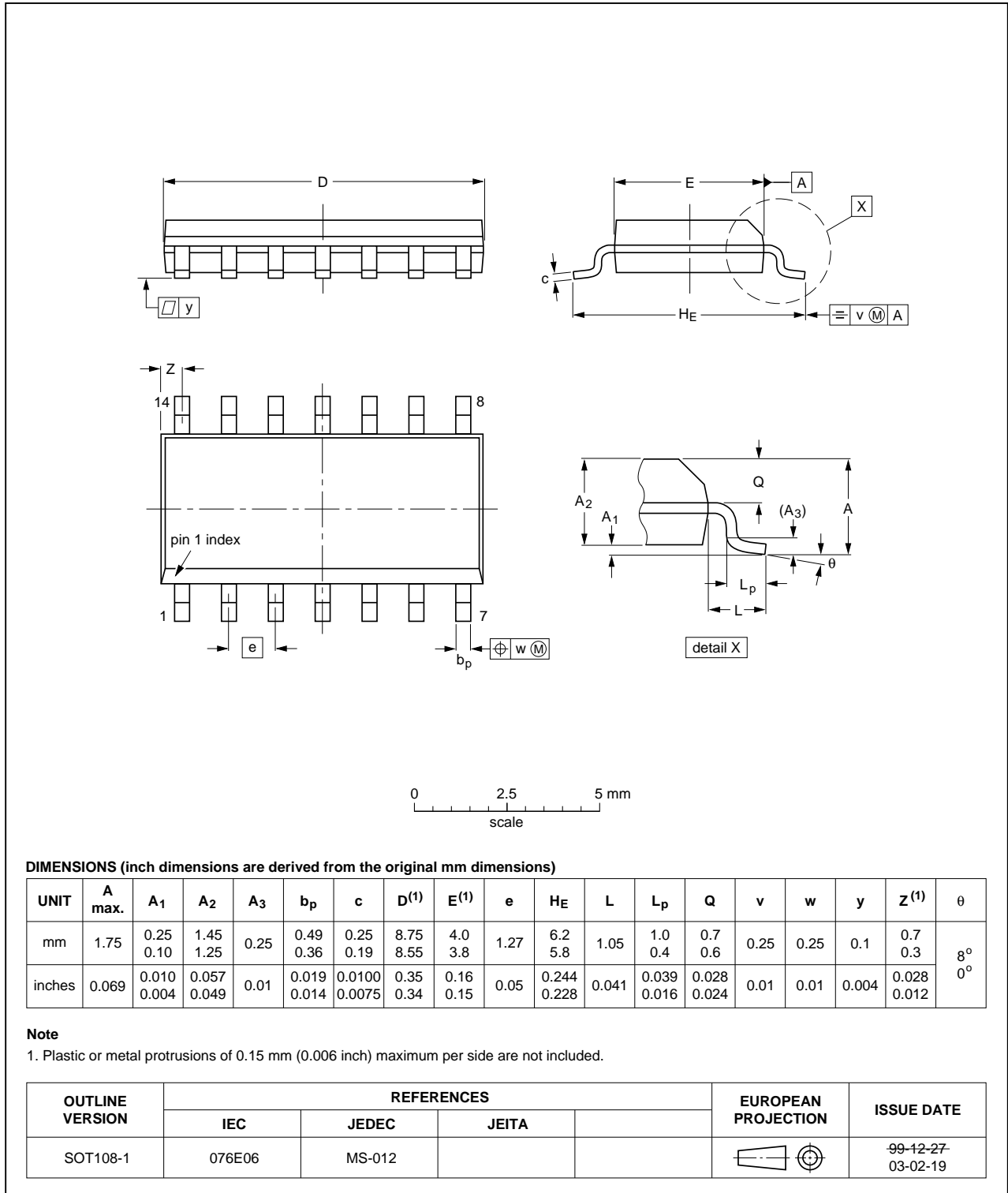


Fig 8. Package outline SOT108-1 (SO14)

## 13. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UBA2212 v.3	20120227	Product data sheet	-	UBA2212 v.2
Modifications:		<ul style="list-style-type: none"><li>• Data sheet status changed from Preliminary to Product.</li><li>• Text and drawings updated throughout entire data sheet.</li></ul>		
UBA2212 v.2	20120209	Preliminary data sheet	-	UBA2212 v.1
UBA2212 v.1	20111209	Objective data sheet	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 14.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 14.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.



**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the

product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

## 14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 15. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 16. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
2.1	System integration .....	1
2.2	General .....	1
2.3	Fast and smooth light out .....	1
2.4	Burner lifetime .....	1
2.5	Safety .....	2
2.6	Ease of use .....	2
<b>3</b>	<b>Applications</b> .....	<b>2</b>
<b>4</b>	<b>Ordering information</b> .....	<b>2</b>
<b>5</b>	<b>Block diagram</b> .....	<b>3</b>
<b>6</b>	<b>Pinning information</b> .....	<b>4</b>
6.1	Pinning .....	4
6.2	Pin description .....	4
<b>7</b>	<b>Functional description</b> .....	<b>5</b>
7.1	Supply voltage .....	5
7.2	Start-up state .....	5
7.3	Reset .....	5
7.4	Oscillation control .....	5
7.5	Preheat state .....	6
7.6	Ignition state .....	6
7.7	Boost state and transition to steady state .....	7
7.8	Steady state .....	7
7.9	Non-overlap time .....	8
7.10	OverTemperature Protection (OTP) .....	8
7.11	Saturation Current Protection (SCP) .....	8
7.12	Capacitive Mode Protection (CMP) .....	8
<b>8</b>	<b>Limiting values</b> .....	<b>9</b>
<b>9</b>	<b>Thermal characteristics</b> .....	<b>9</b>
<b>10</b>	<b>Characteristics</b> .....	<b>10</b>
<b>11</b>	<b>Application information</b> .....	<b>12</b>
<b>12</b>	<b>Package outline</b> .....	<b>13</b>
<b>13</b>	<b>Revision history</b> .....	<b>15</b>
<b>14</b>	<b>Legal information</b> .....	<b>16</b>
14.1	Data sheet status .....	16
14.2	Definitions .....	16
14.3	Disclaimers .....	16
14.4	Trademarks .....	17
<b>15</b>	<b>Contact information</b> .....	<b>17</b>
<b>16</b>	<b>Contents</b> .....	<b>18</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 27 February 2012

Document identifier: UBA2212